Supporting Information

Silicon nanoparticle charge trapping memory cell

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1 Transistor output and gate leakage

The output curve of the transistor is measured by sweeping the drain voltage from 0 up to 8 V at different gate voltages as shown in Fig. S1. The transfer curve does not show a significant sub-threshold swing which can be due to leakage current across the blocking oxide.

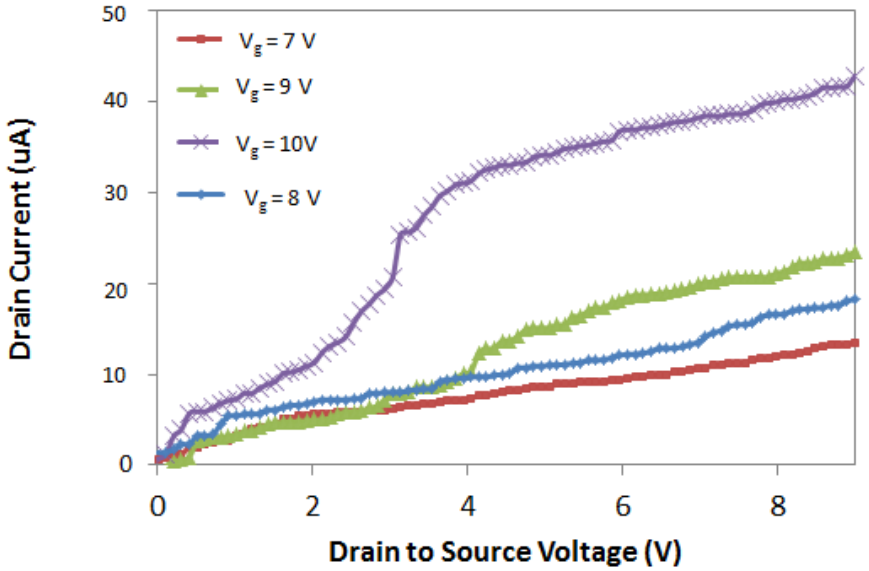

Figure S1 Output curve of the transistor.

In addition, the gate leakage of the transistor is measured by sweeping the gate voltage in the negative and positive sides as shown in Fig. S2 with the drain being grounded and the linear logarithm of the gate current is plotted vs. the gate voltage.

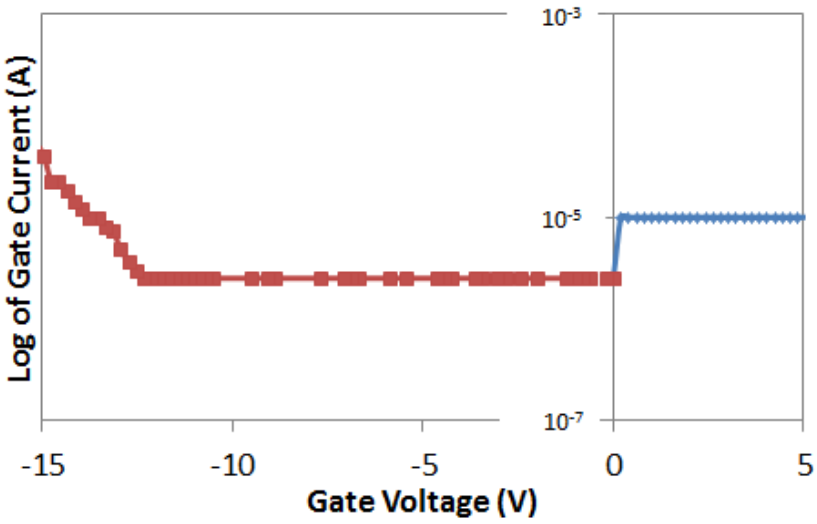

Figure S2 Gate leakage of transistor.

2 TCAD simulations details

The structure is simulated using Synopsys Sentaurus Physics Based TCAD. The memory structure is based on an NMOS structure. The materials properties of ZnO, Al_2O_3 [1-3], and 2 nm Si nanoparticles [4-6] are used. Fowler-Nordheim, phonon assisted tunneling, and direct tunneling were used to model the charge emission mechanism from channel to/from charge storage layer. Size quantization effects are included in all simulations by using the density gradient model. Also, for all simulations, the Lucent mobility model is used and high-field saturation effects are accounted for. The V_t is extracted using the maximum transconductance method. All I-V simulations are performed using the hydrodynamic transport model, where the carrier temperature equation for the dominant carriers – electrons for NMOS–is solved with the electrostatic Poisson equation and the carrier continuity equations. For the high drain bias I_d-V_{gs} simulations, lattice self-heating effects are included by also solving the lattice temperature equation [7]. More details of the simulations can be found in Ref. [7-9].

3 Discussion about the Si nanoparticles size

According to the ITRS roadmap, the charge trapping layer thickness for NAND and NOR charge trapping memory devices should be reduced to 3-4 nm in the coming years. Thus, technologically viable and competitive future devices require the use of sub 3-nm nanoparticles (NPs), 0-D regime, where the electronic structure of Si is modified: larger band gap, smaller dielectric constant, larger work-function, smaller electron affinity, and larger charging energy.

There is no optimal size for the Si NPs, actually, there is a trade-off between some characteristics of the memory based on the size of the NPs. For example, with larger NPs, the electron affinity of the Si is increased which allows mixed electron/holes storage thus the program/erase speed of the memory is expected to increase because of the lighter mass and higher speed of the electrons. However, producing higher density memory devices would become more difficult with thicker charge trapping layers. On the other hand, using small NPs (sub 3-nm) allows for increased memory density. And since the electron affinity is reduced; only holes storage is observed. Therefore, by engineering the valence band offset between channel and tunnel oxide (such as using ZnO channel and Al_2O_3 tunnel oxide as in our case) in order to make the valence band offset smaller than the

conduction band offset (thus holes tunneling probability is much higher than electrons tunneling probability), we can manage to overcome the speed limitations mentioned earlier.

References

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